Listing and Amendments to the Claims

1. (currently amended) A method for multiplying the frame rate of an input video signal comprising the steps of:

~~simultaneously~~ delaying ~~and speeding up~~ successive respective lines of said input video signal to provide a first video signal delayed with respect to said input video signal and speeding up said successive respective lines of said input video signal to provide a second video signal speeded up with respect to said input video signal;

speeding up said first video signal to provide ~~speeded up first~~ a third video signal; and

displaying said input video signal by alternately ~~simultaneously~~ supplying at least one line ~~at least a portion~~ of said second video signal and at least ~~a portion~~ one line of said ~~speeded up first~~ third video signal to ~~separated areas of a liquid crystal~~ display.

2. (previously presented) The method of claim 1, wherein the step of delaying said input video signal includes a step of storing said input video signal in a delay memory.

3. (currently amended) The method of claim 1, comprising the steps of:

periodically interrupting said supplying step to supply a number of consecutive lines of said second video signal;

periodically interrupting said supplying step to supply a number of consecutive lines of said speeded up first video signal; and,

alternating said interrupting steps to maintain a uniform time interval between writing lines into a same line-number position on said ~~liquid crystal~~ display.

4. (currently amended) The method of claim 1, wherein said step of alternately supplying said video signal comprises a the step of alternately writing lines of said video signal to a said ~~liquid crystal on silicon~~ display.

5. (canceled)

6. (currently amended) The method of claim 2, wherein the step of storing said lines of video in said delay memory is carried out by storing less than a full frame of video in said delay memory.

7. (currently amended) The method of claim 1, comprising the steps of:

at least doubling said frame rate of said input video signal; and,

writing selected lines of said video signal multiple times to said ~~liquid crystal~~ display.

8. (previously presented) The method of claim 1, comprising the step of speeding up said first video signal and said input video signal to the same line rate.

9. (currently amended) A method for multiplying the frame rate of a video signal comprising the steps of:

delaying lines of said input video signal for a time less than one a frame period to provide a first video signal delayed with respect to said input video signal;

speeding up said first video signal to provide a ~~speeded up first~~ second video signal;

speeding up said lines of said input video signal to provide a third video signal;

alternately supplying lines of said ~~speeded up input~~ second video signal and lines of said ~~speeded up first~~ third video signal~~; and,~~

~~simultaneously writing said alternately supplied lines into separated areas of~~ to a ~~liquid crystal~~ display.

10. (currently amended) The method of claim 9, comprising the steps of:

periodically interrupting said supplying step to supply a number of consecutive lines of said ~~speeded up input~~ third video signal;

periodically interrupting said supplying step to supply a number of consecutive lines of said ~~speeded up first~~ second video signal; and,

alternating said interrupting steps to maintain a uniform time interval between writing lines into the same line-number position on said ~~liquid crystal~~ display.

11. (currently amended) The method of claim 9, comprising the step of ~~simultaneously~~ alternately supplying ~~writing~~ said lines to top and bottom halves of said display.

12. (original) The method of claim 9, comprising the step of propagating said input video signal through a memory embedded in an integrated circuit.

13. (currently amended) The method of claim 9, comprising the step of speeding up lines of said first video signal and lines of said input video signal to the same line rate.

14. (currently amended) A frame rate multiplier for an input video signal comprising:

a delay memory for delaying lines of said input video signal to provide a first video signal delayed with respect to said input video signal;

a first speed up memory for receiving said lines of said input video signal and for providing a second video signal speeded up with respect to said input video signal;

a second speed up memory coupled to an output of said delay memory for speeding up said first video signal; and

~~means~~ a multiplexer coupled to said first and second speed up memories for ~~simultaneously~~ alternately supplying said first and second video signals to ~~separated areas of~~ a display~~, said means comprising a multiplexer coupled to said first and second speed up memories~~.

15. (previously presented) The frame rate multiplier of claim 14, wherein said delay memory comprises a partial frame memory storing a less than one frame of said video signal.

16. (previously presented) The frame rate multiplier of claim 14, wherein said speed up memory comprises an array of speed up memories.

17. (previously presented) The frame rate multiplier of claim 14 wherein said delay memory comprises an array of memories.

18 - 19. (canceled)

20. (previously presented) The frame rate multiplier of claim 14, wherein said delay memory and said first speed up memory comprise a single memory.

21. (previously presented) The frame rate multiplier of claim 14, wherein said delay memory and said first and second speed up memories comprise a single memory.

22. (canceled)

23. (currently amended) A frame rate doubler comprising:

a first memory for delaying lines of said input video signal to provide a first video signal delayed with respect to said input video signal;

a second memory for speeding up lines of said first video signal;

a third memory for speeding up said lines of said input video signal;

~~means including~~ a multiplexer coupled to said second and third memories for alternately selecting video signals output from said second and third memories for ~~simultaneously~~ writing to ~~separated areas of a liquid crystal~~ said display.

24. (previously presented) The frame rate doubler of claim 23, wherein said first memory stores not more than about 1/2 of a frame said video signal.

25. (currently amended) The frame rate doubler of claim 23, further comprising a controller coupled to said second and third memories and programmed to:

periodically interrupt said supply of said video portions to said ~~liquid crystal~~ display;

supply to said ~~liquid crystal~~ display during said periodic interruptions n successive lines from at least one of said second and third memories so as to maintain a uniform time interval between writing lines into a same line-number position on said ~~liquid crystal~~ display.

26. (currently amended) The frame rate doubler of claim 23, wherein said ~~liquid crystal~~ display is selected from the group comrpising: ~~comprises~~ liquid crystal on silicon and liquid crystal.

27 - 28 (canceled)

29. (previously presented) The frame rate doubler of claim 23, wherein said first and second memories are functionally combined into a single memory.

30 - 31. (canceled)

32. (previously presented) The method of claim 1 including a step of storing in said delay memory not more than a portion of said input signal approximately equal to 1/n of a frame of said input video signal, wherein n represents a multiplying factor for said frame rate multiplier.

33. (previously presented) The frame rate multiplier of claim 14 further comprising a controller coupled to said multiplexer such that said multiplexer is controlled to alternately select a number of successive lines from said first and second speed up memories so as to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display.

34. (new) The frame rate multiplier of claim 1 wherein a frame of said input video signal is displayed by alternately supplying lines of video comprising said frame to a top portion of a liquid crystal display and a bottom portion of said liquid crystal display to display said frame.

35. (new) The frame rate multiplier of claim 34 wherein said frame is displayed by supplying said lines of video first to top and bottom portions of said display before supplying said lines of video to a middle portion of said display.